

15214431102 793591247@qq.com
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FPGA /IC /



2021 09 - 2024 07

2017 09 - 2021 07

(2017-2021);
(2018-2019);

2022 12 - 2023 03

FPGA CE

(1) SPI
(2) flash flash
(3) flash ICAP 25s flash
25 ICAP ICAP 25s
BIN flash
2021 07 - 2021 09



1 Vivado 2019.2 Modelsim Wireshark Matlab Pycharm
2 xc7a100tfgg484-2 FPGA
3
(1) 40ps 25 TDC
(2) FPGA TDC start stop TDC
UDP
(3) FPGA PHY RGMII PHY RJ45
(4) Wireshark UDP
UDP

1 Vivado 2018.2 SDK ModelSim
 2 xc7z020clg400-2 FPGA
 3
 (1) IMX2221 Bayer RGB
 (2) DMA DDR3 PS
 (3) DMA DDR3 hdmi hdmi
 HDMI
 (4) HDMI 60HZ 1080P SD

1 Vivado 2018.2 Modelsim Matlab Wireshark
 2 xc7a75tfgg484-2 FPGA
 3
 (1) Matlab UDP Matlab mat
 (2) RJ45 PHY FPGA PHY RGMII
 (3) FPGA IDDR_CTRL PHY PHY MIG IP
 125MHz 4bit 125x4x2=1000Mbps DDR_CTRL
 HDMI HDMI ODDR_CTRL
 UDP
 (4) HDMI 1024x768@60Hz Wireshark
 UDP CRC

1 Vivado 2018.2 VS2015
 2 xc7a75tfgg484-2 FPGA
 3
 (1) Riffa PCIe PC Riffa API Riffa TLP
 VS2015 MFC Riffa API Riffa
 PC
 API
 (2) Riffa 2 Riffa
 DDR_CTRL MIG IP DDR3 HDMI
 HDMI
 (3) HDMI PC 1080P 800MBps

• 1. Verilog HDL RTL Testbench C/Matlab
 2. FPGA Modelsim ILA ChipScope 3.
 Xilinx ISE Vivado Xilinx Spartan6 Artix7
 4. Linux Spyglass/VCS/Verdi Makefile 5.

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 • CET-6

• 2019.08-2021.7 -

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